

# Room-temperature Wafer Bonder Compatible with 300-mm Wafers for Three-dimensionally Stacked LSIs



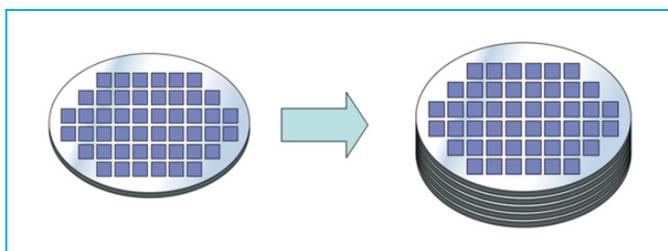
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The limits of miniaturization in the semiconductor manufacturing process have become an issue in recent years. Semiconductor manufacturers have thus far coped with the need for functional enhancement and capacity expansion by miniaturizing devices and wires, but the limits of two-dimensional miniaturization have gradually become obvious. Three-dimensional stacking of semiconductor devices has been promoted as one of the methods to conquer these limitations. This article outlines a 300-mm wafer-compatible room-temperature bonder developed by Mitsubishi Heavy Industries, Ltd. (MHI), which is used to manufacture three-dimensionally stacked large-scale integrated circuits (LSIs).

## 1. Necessity of three-dimensional stacking technique in semiconductor manufacturing

In the field of LSIs such as microprocessors and memory, functional enhancement and capacity expansion have been achieved through the reduction of the size of devices (transistors) and the miniaturization of wiring. According to Moore's law, the number of transistors that are mounted on an integrated circuit doubles approximately every 18 months.

However, there is a limit in transistor size reduction and wiring miniaturization, and this overshadows the capability to promote device development at the same pace as before. This is due to the fact that devices and wires are arranged in two dimensions in an LSI structure. As one of the methods to overcome this limit, it has been suggested to stack wafers provided with devices in three dimensions so that functional and capacity expansion can be achieved while maintaining the same area. The concept of three-dimensional wafer stacking is illustrated in **Figure 1**.

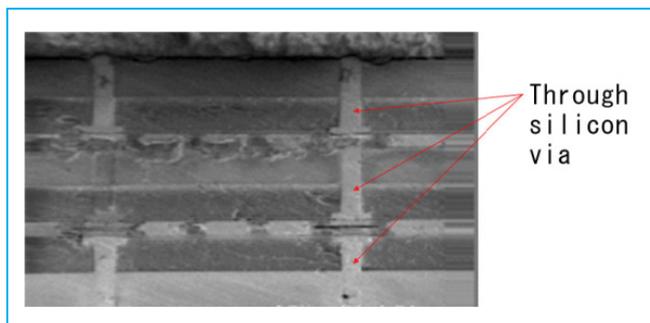


**Figure 1** Schematic diagram of three-dimensional wafer stacking

The following two new techniques are required to stack wafers:

- (1) Formation technique of TSV (Through Silicon Vias) for signal transmission and reception between wafers; and
- (2) Technique to bond wafers while connecting the TSV.

**Figure 2** shows an example of TSV. The 300-mm compatible room-temperature wafer bonder outlined in this article is an apparatus to provide bonding between wafers, as mentioned in item (2) above.



**Figure 2 Example of through silicon vias**  
(Courtesy of Yole Development)

## 2. Characteristics of 300-mm wafer-compatible room-temperature bonder

Room-temperature bonding is a technique to remove the oxide film and absorbed substances on wafer surfaces by irradiating the wafers with ions or neutral atoms of an inert element in a high vacuum so that the activated surfaces can be bonded. The process has the following characteristics:

- (1) Since the process requires no heating, the wafers are free from thermal strain. The process can also increase yield because it causes no thermal stress on the devices on the wafers.
- (2) Since the process requires no heating, it enables highly precise alignment ( $\pm 2 \mu\text{m}$ ) between bonded wafers, even when bonding wafers with different thermal expansion coefficients.
- (3) The process is applicable to bond a wide range of materials including silicon-based materials and metals. It is also capable of bonding the TSV of various materials.
- (4) Since the process requires no heating or cooling, it has high throughput.

For the efficient removal of oxide films on the TSV to be bonded, the bonder uses high energy fast atom beams (FAB) to activate the wafer surfaces. By determining the optimum arrangement of multiple FAB guns through digital simulations, the bonder has achieved high productivity.

## 3. Specifications

Specifications for the bonder are listed in **Table 1**. The bonder is fully automated. By simply placing five sets (10 pieces) of wafers in a wafer cassette, wafer transfer, alignment (positioning of wafers to be bonded) and other tasks are all carried out without manual operation. In addition, the bonder is capable of pressing the wafers with a high pressing load (200 kN) to provide stable bonding. Although the running cost usually poses a problem in device mass production, the bonder allows for an extremely low running cost because it only requires inexpensive, safe utilities such as argon gas, nitrogen gas, cooling water, and compressed air. The bonder is also designed with due consideration for maintainability, thus allowing easy maintenance work.

**Table 1 Main specifications**

Unit of operation	5 sets (max.)
Wafer size	300 mm/200 mm
Operation mode	Fully automatic
Alignment accuracy	$\pm 2 \mu\text{m}$ (measurement by MHI)
Surface activation	Argon fast atom beam
Press unit	Max. load: 200 kN
Alignment	IR transparent image
Degree of vacuum in chamber	$1.0 \times 10^{-5}$ Pa
Utilities	Argon gas, nitrogen gas, compressed air, cooling water, power supply (200/100 V)

## 4. Field of application

With the rapid spread of smartphones and mobile terminals, the need for smaller devices is increasing and demand for shorter product development cycles is also intensifying. To meet such needs, the three-dimensional stacking technique is expected to be applied to the following devices:

(1) Memory

Capacity can be increased by more than 10 times while maintaining the equivalent device footprint.

(2) Microprocessors

Microprocessors are devices for which functional integration is being maximized. However, by allocating functions thus far integrated in a single device and stacking them in three dimensions on the basis of function, functional expansion can be achieved while keeping the area unchanged.

Existing microprocessors require overall circuit modification when part of the functionality is changed. With the use of the three-dimensional stacking technique, it is only necessary to modify the devices on the layer relevant to the change, thus shortening the development cycle.

(3) Micro electro mechanical systems (MEMS)

With the three-dimensional integration of mechanical elements, such as acceleration and pressure sensors and signal and information processing elements, devices can become more sophisticated and at the same time, further reduction in size and improvement in reliability can be anticipated.

We intend not only to further improve the bonder as a manufacturing apparatus to meet such needs, but also to focus on the rapid spread of three-dimensionally stacked LSIs by supporting the bonding process in customer device development.