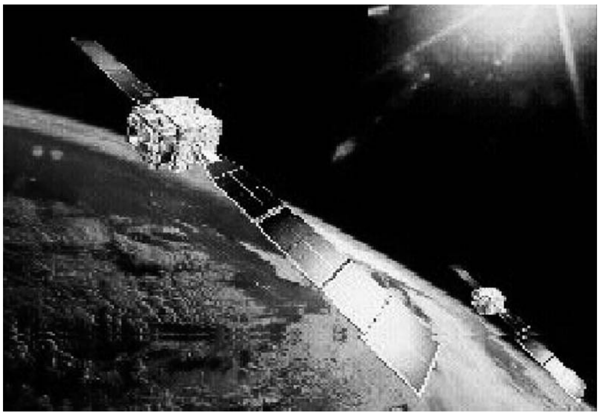

# Space Verification of On-Board Computer Integrated with Commercial IC

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*Positive use of Commercial Off-The-Shelf (COTS) device and commercial technologies for space application have become important in reducing cost and improving the performance of small satellite-borne devices. Mitsubishi Heavy Industries, Ltd. (MHI) has developed a low-cost, high-performance On-Board Computer (OBC) for satellites with COTS parts and technologies, and has conducted space verification tests since November 2003 using Space Environment Reliability Verification Integrated System (SERVIS) #1. Excellent verification has been observed for 2 years in space. We introduce the OBC and space verification test results.*

## 1. Introduction

High demands for communication and observation satellites have necessitated the development of small low-cost high-performance satellite-borne electronic equipments to build a global network in the 21st century.

Conventional equipments for satellites are composed of special high-reliability parts that are expensive and is several generations older than that of the most advanced commercial parts in the technology. The use of COTS parts and technology and their application in space have thus become a key means for reducing costs and realizing small high-performance equipments.

However, COTS parts are not designed for use in severe environments in space, and have problems with radiation tolerance and environment resistance (vibration, heat, etc.) No data from parts manufacturers guarantees against radiation (although those data are required in equipment design), and no evaluation of radiation tolerance in orbit has been established, leaving many problems unsolved.

MHI developed a low-cost, high-performance OBC using COTS parts after solving these problems and applying them in space. We have been conducting space verification tests on SERVIS-1.

## 2. Development of experimental equipment

### 2.1 Specifications

This OBC will be used as satellite-borne equipment. Its development specifications shown in **Table 1** are determined to meet processing requirements for the equipment in the future. To realize image processing, etc., the processing performance was set at 100 MIPS or over – 10 times that of equipment for conventional satellites. Different radiation measures in item 2.3 have been taken and radiation tolerance evaluation circuits for COTS parts have been added. **Fig. 1** shows the new OBC.

**Fig. 1 OBC**

**Table 1 Development specifications**

| Item | Performance and general item |
|---|---|
| CPU | 32 bit CPU |
| Processing performance | 100 MIPS (1 million commands/s) or over |
| Memory size | SRAM (1 Mbyte), SDRAM (16 Mbyte) |
| Power consumption (Typ) | 20 W |
| Outside dimensions (Typ) | 302 x 230 x 84 mm |
| Weight (Typ) | 5.2 kg or less |
| Additional functions | Radiation tolerance circuit, part evaluation circuit |

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### 2.2 COTS parts and technology

We used the 6 high-performance COTS parts in **Table 2** for the computer key parts (CPU, memory, etc.) partly because they are expected to reducing their costs, to improve their performance, and to decrease their sizes, and partly because they are found to be useful in assessing tolerance for space applications from ground radiation test results.

We adopted Multi-Chip-Module (MCM) mounting technology (commercial technology) that is effective for the equipment to improve its ruggedization in harsh environment, reducing its cost, and decreasing its size.

COTS parts (with bare silicon chips) are mounted on a ceramic package equivalent in size to a name card (55 x 95 mm). This enabled us to realize low cost and downsized equipment to one-fifth the conventional size of general-purpose CPU boards.

**Fig. 2** shows the CPU-MCM.

### 2.3 Disadvantages of COTS parts and corrective measures

The low-cost high-performance COTS parts have problems for use in orbit such as radiation tolerance and environment resistance (vibration, heat, etc.). Different radiation in orbit such as heavy ions from outside the solar system, protons from the sun, and protons trapped in geomagnetic fields cause electronic parts to malfunction and permanent damage, then it is necessary for electronic parts to take corrective action. Parts must be evaluated for tolerance of radiation as follows:

(1) Single-event Upset

Single-event upset (SEU) occurs when a single proton or heavy ion enters a part, inverting binary 1s 0s and causing provisional malfunctions. The test parameter is the rates of upsets errors.

(2) Single-Event Latchup

Single-even latchup (SEL) occurs when a single proton or heavy ion enters a part, causing overcurrent called latchup that permanently damages the part. The test parameter is the evaluation of latchup occurrence.

(3) Total Ionizing Dose

In total ionizing dose (TID), irradiation from accumulated electrons and protons increases the leak current, causing devices to function abnormally. The test parameter is the evaluation of current fluctuation and the presence of functional abnormalities.

To improve ruggedization in harsh environment including that of radiation, we took the corrective action in **Table 3**, making COTS parts more reliable in space applications.

**Table 2 COTS parts**

| Type | Function |
|---|---|
| CPU | 32 bit RISC CPU |
| SDRAM | 64M bit memory |
| SRAM | 4M bit memory |
| Gate Array | 32 000 gate FPGA |
| Digital IC1 | 16 bit bus transceiver |
| Digital IC2 | RS-422 driver |

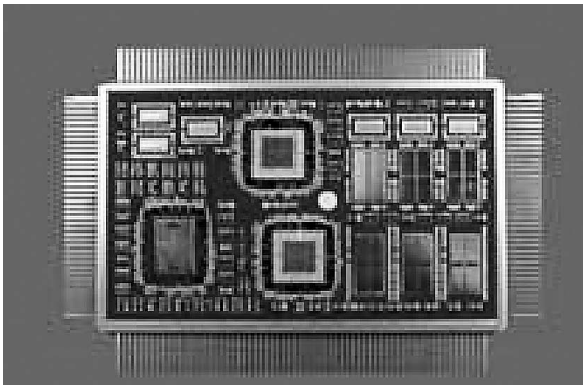

**Fig. 2 CPU-MCM (55 X 95mm)**

**Table 3 Measures used in OBC**

| Measure | Purpose |
|---|---|
| Memory error detection and corrective circuit against SEU | Circuit for detecting up to 2 bit errors and correcting 1 bit errors |
| Redundancy against SEU | Redundancy for backup when 2 CPU malfunctions, improving reliability. |
| Watchdog timer against SEU | Checking that the CPU conducts specified processing in a constant interval and detecting CPU malfunctions to restart and reset it. |
| Overcurrent detection circuit against SEL and TID | Detecting overcurrent in parts and protecting parts from burning by cutting off current. |
| MCM mounting for small, ruggedization and low cost | High-density mounting on bare IC in one ceramic or metallic package, effective in downsizing.<br>Since technology improves resistance to vibration, humidity, and heat of a resin package, it contributes to simultaneously realizing improved ruggedization in a harsh environment and low cost by using COTS parts. |

### 2.4 Experimental equipment configuration

The equipment configuration is shown in **Fig. 3**. This redundant system (A and B) is broadly divided into two functional parts - CPU circuits with CPU-MCM and the power supply unit. The OBC has a 3-stage structure of the following parts.

- CPU circuit (Systems A/B): One stage each
- Power circuits: One stage (two power supply units)

The space verification test items for the OBC involve CPU operation - simulated flight control, imaging, and performance evaluation (MIPS), and current consumption – mainly the evaluation of radiation effects.

## 3. Space verification test results

The OBC on SERVIS-1 was launched on October 30, 2003, and has been undergoing space verification testing under a two-year project in an orbit inclined 100 deg at an altitude of 1 000 km. The results thus far have been excellent. The verification testing is conducted at two levels – equipment and part levels – automatically in orbit before the results are transmitted through the satellite and stored on the ground. The results obtained at the start of operation (November 2003) through July 2005 are given below.

### 3.1 Equipment evaluation test results

The space verification test results for equipment level are given in **Table 4**. Simulated operations have been normal since the satellite was launched, with CPU processing performance 110 MIPS, higher than the development specification of 100 MIPS.

The functions added as measures against radiation are operating normally, with memory errors detected and corrected 9 times.

### 3.2 Parts evaluation test results

The evaluation results for part level obtained in the verification tests below were studied and compared to the predicted tolerances calculated based on the ground radiation test results for each COTS part conducted before the satellite was launched.

(1) SEU and SEL evaluation

The rates of SEU are evaluated in **Table 5**. The SEU rate was calculated in 3 steps. First, the environment of radiation was calculated through simulation for each orbit. Second, the environment of radiation was calculated after shielding of the satellite and OBC case. Third, the tolerance of radiation (cross section data from ground radiation tests) was used to calculate the predicted SEU rate.

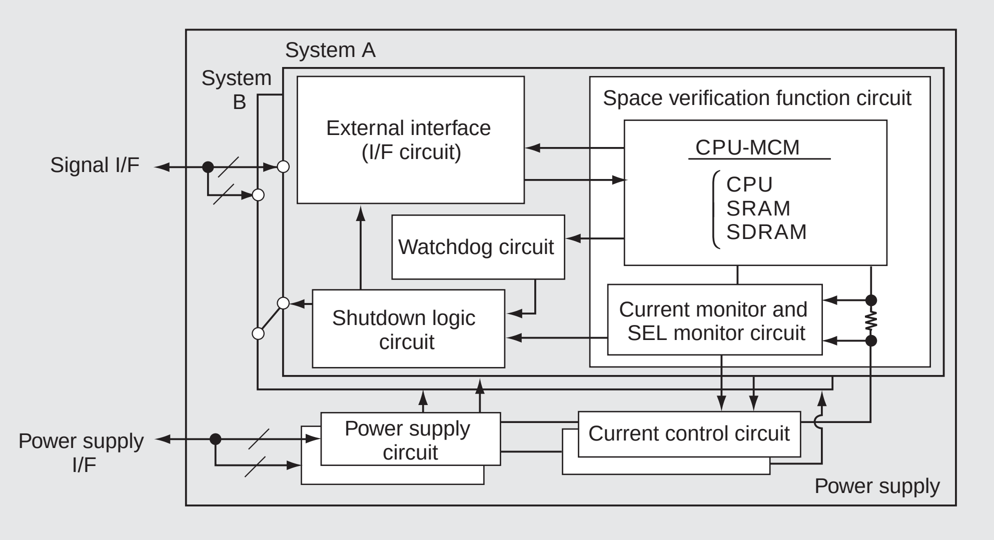

Fig. 3 Functional configuration (redundancy with Systems A and B)

Table 4 Space verification test results (equipment level)

| Evaluation items and results, including evaluation measures against radiation |
|---|
| 1. Simulated flight control operation<br>→ Normal operation with no abnormal functions due to radiation |
| 2. Simulated image data processing operation<br>→ Normal operation with no abnormal functions due to radiation |
| 3. Performance evaluation of CPU operation<br>→ Operation at 110 MIPS |
| 4. Measures against radiation<br>→ Confirmation of memory error detection and corrective circuit effectiveness |

**Table 5 SEU results [Compared in (1) - (3)]**

| COTS parts | | Prediction based on ground test results | | Observed results in orbit |
|---|---|---|---|---|
| Analytical conditions | | Radioation environment by simulation (CREME) | Radioation environment measured in orbit (July 2005) | — |
| | | Shielding: Calculation of radiation environment after shielding of satellite and OBC case | | • Error rate observed on the satellite (July 2005)<br>• Proton-caused error dominant |
| | | Cross section: Proton SEU cross section derived from Heavy Ion | | |
| | | SEU rate (1) | SEU rate (2) | SEU rate (3) |
| CPU | Command cache | 0.08 times/day | 0.5 times/day | 0.5 times |
| | Data cache | 3.87 times/day | 27 times/day | 0.21 times/day |
| SRAM | | 17 times/day | 117 times/day | 4.0 times/day |
| SDRAM | | 16.7 times/day | 109 times/day | ≒0 times/day |
| Gate Array | | ≒0 times | ≒0 times | 0 times |
| Digital IC 1 | | ≒0 times | ≒0 times | 0 times |
| Digital IC 2 | | ≒0 times | ≒0 times | 0 times |

(1) and (2) in Table 5 indicate the predicted SEU error rate based on the ground radiation test results for the parts and (3) indicates the actual error rate observed in orbit. In calculating (2), we used the data measured using radiation sensors on the satellite as a reference for calculating environment of radiation in the step 1.

The results show that SEU occurs in 3 of the 6 types, with error rate in each case lower than the predicted result based on the ground evaluation test results, with error rate for the CPU and SRAM being 1/4 and for SDRAM 1/17.

Almost of errors were centered on the South Atlantic Anomaly (SAA) where the geomagnetic field is degraded, causing large amounts of protons to be trapped even at low attitudes (**Fig. 4**).

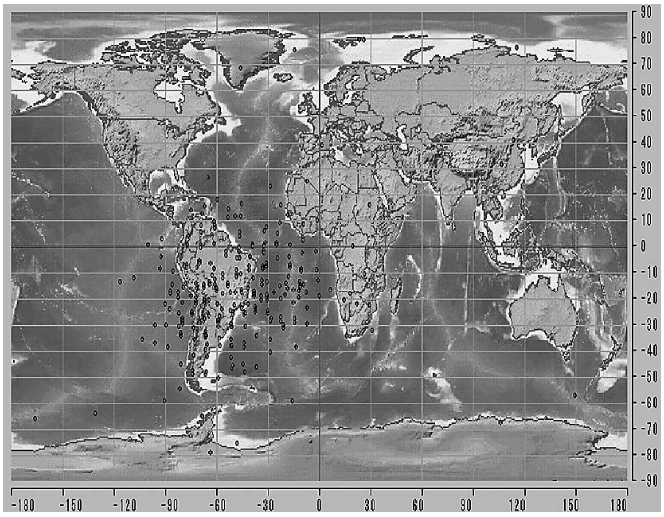

**Fig. 4 SEU map for 4M SRAM**

The radiation particulates observed in orbit were protons (100 – 500 [1/(cm$^2$-sr-s)]) and heavy ions (0.1 [1/(cm$^2$-sr-s)]). Protons are clearly main cause of errors.

For SEL, no latchup was found for any of the six types, as predicted from the ground evaluation tests.

(2) TID results

The TID results (**Table 6**) showed the obtained TID to be lower than that predicted, i.e., 70% of predicted values. No change was seen in current consumption for any of the 6 types, and no functional abnormality was detected. All parts are thus assumed to have a TID tolerance exceeding 1.7 krad (Si) [unit of absorbed radiation dose versus (Si)]. Since each part has been found through the ground evaluation tests to have a tolerance 10 times this level, there appears to be no problem in the current mission.

**Table 6 TID results**

| COTS parts | Comparison of TID calculated after shielding | |
|---|---|---|
| | Predicted based on environmental simulation | Observed in orbit (as of end of July 2005) |
| All 6 COTS parts | 2.5 krad (Si)<br>(3.8 rad/day) | 1.7 krad (Si)<br>(2.6 rad/day) |

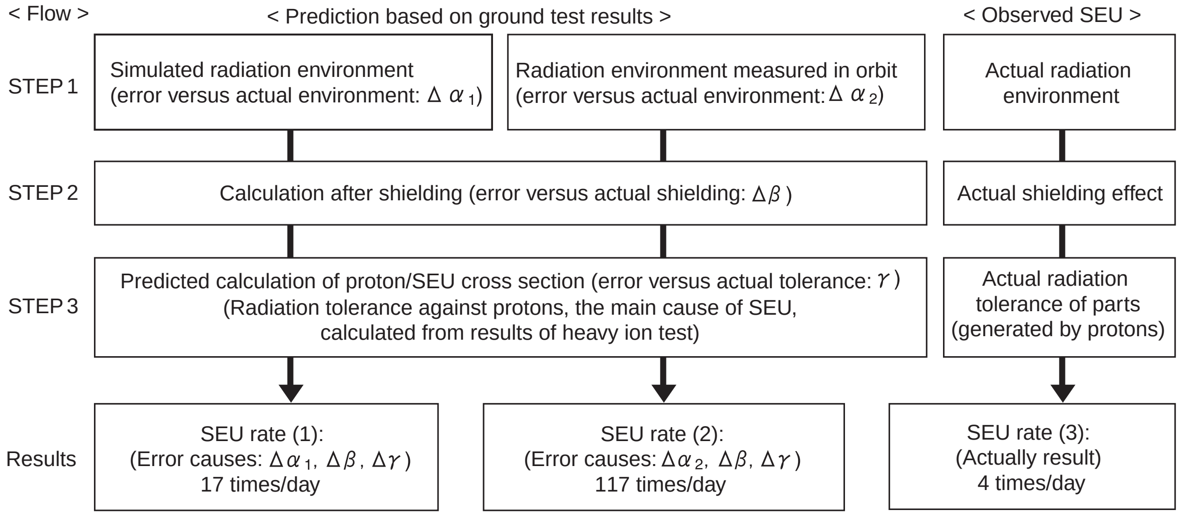

**Fig. 5 Flow of SEU calculation and error causes (e.g., SRAM)**

### 3.3 Consideration of space verification test results

The space verification test results have thus far been normal in different operations in equipment, with operating performance higher (110 MIPS) than development specifications. The space operation records obtained during 2 years show bright prospects for high reliability of COTS parts in space use (Table 3).

The radiation tolerance data for all 6 parts was obtained through the space verification tests, ensuring the applicability of parts to medium and low orbits in space.

In predicting SEU rate, an important aspect of design, we considered error-causing factors while predicting radiation tolerance in orbit.

**Fig. 5** shows SEU rate calculation and compares error-causing factors for SEU rate (1) – (3). These factors were deduced from evaluation test results on the ground and in orbit based on the flows – summed up as follows:

- Errors due to differences between calculated and actual radiation environments ( $\Delta\alpha_1$, $\Delta\alpha_2$ )
- Calculation errors after shielding ( $\Delta\beta$ )
- Prediction errors in radiation tolerance of parts due to protons ( $\Delta\gamma$ )

Actual measurements of the radiation environment, the first error-causing factor, was one digit higher than predicted, possibly attributable to error in environmental measurement or error in environment simulation models. The second error-causing factor, error in calculating after shielding, may lie in shielding model between outer space and parts on OBC or the attenuation calculation code. Errors in prediction of part radiation tolerance due to proton may lie in tolerance conversion models from heavy ions on the ground to protons, the main cause of SEU.

We must thus improve the accuracy of radiation tolerance prediction by studying causes of the above error-causing factors.

## 4. Conclusions

The successful record for about 2 years of the On-Board Computer (OBC) developed for application to satellites and the COTS parts on the OBC show bright prospects for space application of the COTS parts. The following achievements were obtained in the application of COTS parts and technologies to space:

(1) Verification of the effects of using high-performance COTS parts and MCM technology.
- Realization of reducing cost – one-third that of conventional equipment (one-fifth using MCM).
- Realization of high performance over 10 times higher than that of a conventional CPU boards.
- Realization of downsizing – one-fifth that of conventional boards (name-card-sized MCM)

(2) Acquisition of know-how for improving ruggedized tolerance and high reliability.

(3) Acquisition of know-how on radiation tolerance evaluation and prediction.

MHI is continuing to collect evaluation data in space verification tests to improve data reliability. We thank those at New Energy Development Organization (NEDO) and Institute for Unmanned Space Experiment Free Flyer (USEF) for their guidance and advice in developing OBC.


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